

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**5    Listing of Claims:**

Claim 1 (currently amended) A parasitic capacitance-preventing dummy solder bump structure, the dummy solder bump structure being formed on a substrate, the dummy solder bump structure comprising:

- 10        at least one conductive layer formed on the substrate;  
         a dielectric layer formed on the substrate to cover the conductive layer;  
         a passivation layer formed on the dielectric layer to completely cover the dielectric layer;  
         an under bump metallurgy layer (UBM layer) directly formed on the dielectric  
15        layer surface of the passivation layer without a metal pad there in between ; and  
         a solder bump formed on the UBM layer.

Claim 2 (currently amended) The dummy solder bump structure of claim 1 wherein the substrate is a semiconductor wafer with circuits formed inside the  
20        semiconductor wafer, ~~and the dielectric layer comprises at least one deposition layer formed by a chemical vapor deposition (CVD) process and employed as a passivation layer.~~ and the passivation layer is formed by a chemical vapor deposition (CVD) process.

25        Claim 3 (currently amended) The dummy solder bump structure of claim 2 [[1]] wherein the ~~deposition~~ dielectric layer and the passivation layer comprise ~~comprises~~ either silicon nitride or silicon oxide.

Claim 4 (original) The dummy solder bump structure of claim 1 wherein the UBM  
30        layer is a metal layer formed by a sputtering process.

Claim 5 (currently amended) The dummy solder bump structure of claim 1 wherein a plurality of solder bump structures is formed on the ~~dielectric~~ passivation layer.

5 Claim 6 (currently amended) The dummy solder bump structure of claim 5 wherein each of the solder bump structures comprises:  
a metal pad formed on the ~~dielectric~~ passivation layer;  
an UBM layer formed on the metal pad; and  
a solder bump formed on the UBM layer.

10 Claim 7 (original) The dummy solder bump structure of claim 6 wherein each of the solder bump structures comprises at least one via plug for electrically connecting the solder bump structure with a corresponding portion of the conductive layer below the solder bump structure.

15 Claim 8 (original) The dummy solder bump structure of claim 5 wherein the solder bump structure is positioned in a central area of a surface of the substrate, and the dummy solder bump structures are positioned in a border area of the surface of the substrate to surround at least one of the solder bump structures.

20 Claim 9 (original) The dummy solder bump structure of claim 1 wherein the dummy solder bump structure is employed to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

25 Claim 10 (currently amended) A method of forming a solder bump on a substrate, the substrate comprising at least one conductive layer positioned on a surface of the substrate, the surface of the substrate comprising a first area and a second area, the method comprising:

performing a CVD process to form a dielectric layer on the substrate to cover the conductive layer;  
30 forming a passivation layer on the surface of the dielectric layer to completely cover the dielectric layer;

forming at least one via plug only in portions of the dielectric layer and the passivation layer within the first area down to a surface of the conductive layer;

forming at least one metal pad only in portions of the ~~dielectric~~ passivation layer within the first area, the metal pad being electrically connected to the via plug;

- 5 performing an UBM process to form at least one UBM layer ~~to cover both~~ on the metal pad within the first area and at least one UBM layer directly on to cover portions the surface of the dielectric layer passivation layer without a metal pad there in between within the second area; and

forming a solder bump on each of the UBM layers.

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Claim 11 (canceled).

Claim 12 (currently amended) The method of claim ~~11~~ 10 wherein the dielectric layer and the passivation layer comprise either silicon nitride or silicon oxide.

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Claim 13(original) The method of claim 10 wherein the via plug comprises either one of titanium (Ti), titanium nitride (TiN), tungsten (W), aluminum (Al), copper (Cu) or copper-aluminum alloy (Cu-Al alloy).

- 20 Claim 14 (original) The method of claim 10 wherein the UBM layer is formed by performing a sputtering process.

Claim 15 (original) The method of claim 10 wherein the solder bump formed within the second area is employed as a dummy solder bump to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

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Claim 16 (original) The method of claim 10 wherein the substrate is a semiconductor wafer with circuits formed inside the semiconductor wafer.

- 30 Claim 17 (original) The method of claim 10 wherein the first area and the second area are respectively a central area and a border area of the surface of the substrate.

Claim 18 (previously presented) The dummy solder bump structure of claim 1  
wherein the UBM layer dose not contact with the conductive layer.

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